WHAT IS CLAIMED IS:

1. A method for manufacturing a MOSgated device comprising:

providing a semiconductive body of a first conductivity type;

forming spaced insulating bodies of a first thickness over a first major surface of said semiconductive body;

forming an insulation layer of a second thickness over said first major surface in areas between said spaced insulating bodies, said second thickness being thinner than said first thickness;

forming a gate electrode on at least one side of each of said spaced insulating bodies, each gate electrode being disposed over at least a portion of a respective insulation layer;

forming a body region of a second conductivity type in said semiconductive body; and

forming regions of said first conductivity type in said body regions, each said regions of said first conductivity type being spaced from said semiconductive body by a channel region in said body region, said channel region being disposed under a respective insulation layer.

2. A method according to claim 1 further comprising, implanting dopants of said second conductivity type below said body region and diffusing the same to form deep junctions extending below said body regions into said semiconductive body.

3. A method according to claim 2, wherein said deep junctions are formed by at least two implant steps each at a different implant energy.

4. A method according to claim 1, wherein each spaced insulating body includes at least two vertical sidewalls, and further comprising forming a respective gate electrode adjacent each sidewall of an insulating body.

5. A method according to claim 4, wherein said gate electrodes are formed to be connected to one another.

6. A method according to claim 1, further comprising forming a layer of silicide on a side wall of each of said gate electrodes.

7. A method according to claim 6, wherein said silicide is comprised of WSi.

8. A method according to claim 1, further comprising forming insulation over said gate electrodes.

9. A method according to claim 1, further comprising forming a contact layer over said spaced insulating bodies and said gate electrode, said contact layer being formed through said regions of said first conductivity type and in contact with said body regions.

10. A method according to claim 1, further comprising forming an oxidation prevention layer on portions of said gate electrodes and said insulation layers, and oxidizing portions of said gate electrode not covered by said oxidation prevention layer.

11. A method according to claim 10, wherein said oxidation prevention layer is comprised of a nitride.

12. A method for manufacturing a MOSgated device comprising:

providing a semiconductive body of a first conductivity type;

forming a body region of a second conductivity type in said semiconductive body;

forming regions of said first conductivity type in said body regions, each said regions of said first conductivity type being spaced from said semiconductive body by a channel region in said body region; and

implanting dopants of said second conductivity type below said body region and diffusing the same to form deep junctions extending below said body regions into said semiconductive body.

13. A method according to claim 12, wherein said deep junctions are formed by at least two implant steps each at a different implant energy.

14. A method according to claim 12 further comprising, forming spaced insulating bodies of a first thickness over a first major surface of said semiconductive body;

forming an insulation layer of a second thickness over said first major surface in areas between said spaced insulating bodies, said second thickness being thinner than said first thickness;

forming a gate electrode on at least one side of each of said spaced insulating bodies, each gate electrode being disposed over at least a portion of a respective insulation layer.

15. A method according to claim 14, wherein each spaced insulating body includes at least two vertical sidewalls, and further comprising forming a respective gate electrode adjacent each sidewall of an insulating body.

16. A method according to claim 15, wherein said gate electrodes are formed to be connected to one another.

17. A method according to claim 14, further comprising forming a layer of silicide on a side wall of each of said gate electrodes.

18. A method according to claim 17, wherein said silicide is comprised of WSi.

19. A method according to claim 14, further comprising forming insulation over said gate electrodes.

20. A method according to claim 14, further comprising forming a contact layer over said spaced insulating bodies and said gate electrode, said contact layer being formed through said regions of said first conductivity type and in contact with said body regions.

21. A method according to claim 14, further comprising forming an oxidation prevention layer on portions of said gate electrodes and said insulation layers, and oxidizing portions of said gate electrode not covered by said oxidation prevention layer.

22. A method according to claim 21, wherein said oxidation prevention layer is comprised of a nitride.

23. A process for manufacturing a MOSFET device comprising:

providing a substrate of a first conductivity type having an epitaxial layer of the same conductivity type formed on a top surface thereof;

forming base regions of a second conductivity type in said epitaxial layer;

forming source regions of said first conductivity type in said base regions;

forming deep junctions of said second conductivity type under said base regions by multiple implants of dopants of said second conductivity type.

24. The process of claim 23, wherein said deep junctions are one of as thick as said epitaxial layer and at least twice as thick as said base regions.